



LTPS-LCD BIAS POWER SUPPLY, TRIPLE CHARGE PUMP

FEATURES

- Complete LTPS-LCD Bias Solution
- Triple Output Charge Pump Providing V_{CC} at 16 mA, V_{DD} at 2 mA, V_{SS} at 1 mA
- 2.4 V to 5.5 V Input Voltage Range
- Fixed Output Voltages of 3.3 V, 7.5 V, -2.7 V or 5.0 V, 9.0 V, -3.0 V
- 50 μ A Typical Quiescent Current
- Less Than 1 μ A Shutdown Current
- Ultra-Low Ripple ($V_{CC} = 5$ mV, Typical at 5 mA)
- Autonomous Boost for V_{CC} Supply
- 1.5% Accuracy on Fixed V_{CC} Output Voltage
- Sequential Power Control
- 24-Pin QFN Package (4 x 4)

APPLICATIONS

- Small Form LTPS-LCD Displays
- PDAs, Pocket PCs
- Smart Phones

DESCRIPTION

The TPS65110/11 is a very compact power supply solution providing the three voltages required by many LTPS LCD displays.

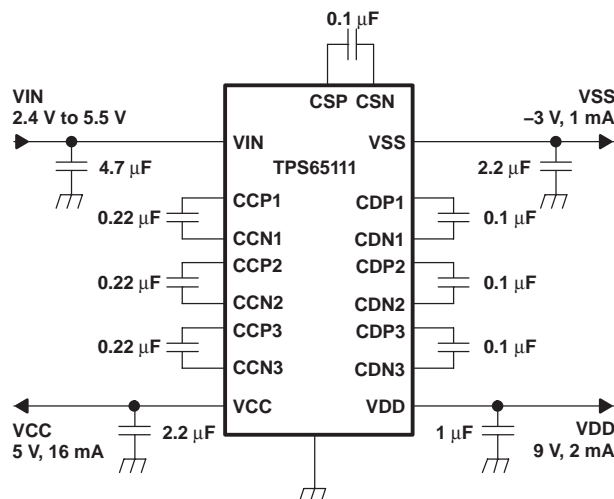
All three regulated outputs are generated using a charge pump topology.

The V_{CC} charge pump provides precise, high efficiency, and very low ripple dc/dc conversion for the LCD analog power. The V_{CC} boost ratio (x1.0, x1.33, x1.5, and x2.0) is automatically set based on input and output voltage conditions. The V_{CC} output assures 16 mA of current by using three 0.22- μ F flying capacitors. If the required output current is smaller, smaller capacitors can be applied.

The V_{DD} charge pump provides a higher positive voltage, and the V_{SS} charge pump provides the negative output voltage. Power up/down sequences are internally set and are secured even in cases of sudden and abnormal V_{IN} drop.

One of the most significant features of the TPS65110/11 is the ultra-low output voltage ripple, as the V_{CC} charge pump achieves 5-mV output ripple voltage.

APPLICATION CIRCUIT FOR TPS65111



AVAILABLE OUTPUT VOLTAGE OPTIONS

| PART NUMBER | V_{CC} | V_{DD} | V_{SS} | V_{DD} BOOST |
|-------------|----------|----------|----------|----------------|
| TPS65110RGE | 3.3 V | 7.5 V | -2.7 V | X3 |
| TPS65111RGE | 5.0 V | 9.0 V | -3.0 V | X2 |

- (1) The RGE package is available in tape and reel.
Add R suffix (RGER) to order quantities of 3000 parts.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

| | UNIT |
|--|-----------------------|
| Supply voltage at VIN (2) | -0.3 V to 7.0 V |
| Input voltage at EN, CLK, DATA (2) | -0.3 V to VIN + 0.3 V |
| Power dissipation (3) | 46°C/W |
| Virtual operation junction temperature, T _J | -40°C to 125°C |
| Storage temperature range | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

(3) The package thermal impedance is calculated in accordance with JESD 51-5.

CHANNEL PERFORMANCE OVERVIEW

| CHANNEL | VCC | VDD | VSS |
|------------------------|----------------------|-----------|-----------|
| Output Voltage Control | Regulated | Regulated | Regulated |
| Boost Ratio | x1; x1.333; x1.5; x2 | x2 or x3 | x-1 |
| Boost setting | Autonomous Boost | Fixed | Fixed |
| Power Supply | VIN | VCC | VCC |
| Output Current | 16 mA | 2 mA | 1 mA |
| Accuracy | ±1.5% | ±3% | ±3% |
| Num of Ext CAP | 4 | 4 | 2 |

RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|--|------|------|------|------|
| Input voltage range, VIN | 2.4 | | 5.5 | V |
| Main output voltage, V _{CC} | 3.0 | | 5.2 | V |
| Positive output voltage range, V _{DD} | 6.5 | | 10 | V |
| Negative output voltage range, V _{SS} | -4.5 | | -2.4 | V |
| VIN input capacitor(C _i) | | 4.7 | | μF |
| V _{CC} output capacitor(C _{CO}) | | 2.2 | | μF |
| V _{DD} output capacitor(C _{DO}) | | 1.0 | | μF |
| V _{SS} output capacitor(C _{SO}) | | 2.2 | | μF |
| V _{CC} flying capacitors(C _{C1} , C _{C2} , C _{C3}) | | 0.22 | | μF |
| V _{DD} and V _{SS} flying capacitors(C _{D1} , C _{D2} , C _{D3} , C _S) | | 0.1 | | μF |
| Operating ambient temperature, T _A | -40 | | 85 | °C |
| Operating junction temperature, T _J | -40 | | 125 | °C |

ELECTRICAL CHARACTERISTICS

 over recommended free-air temperature, typical at an ambient temperature of 25°C, at $C_{C1}=C_{C2}=C_{C3}=0.22\ \mu\text{F}$, $C_{D1}=C_{D2}=C_{D3}=C_S=0.1\ \mu\text{F}$, $C_{C0}=C_{S0}=2.2\ \mu\text{F}$, $C_{D0}=1.0\ \mu\text{F}$, $V_I=3.6\ \text{V}$, and default output voltages (unless otherwise noted)

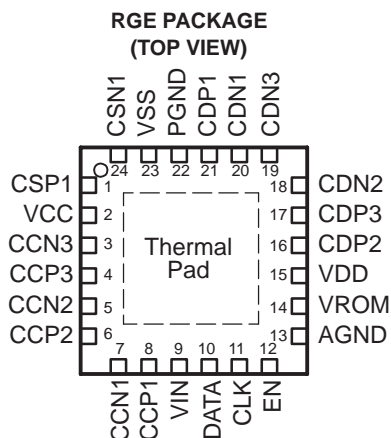
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------------------------------------|---|-------|------|-------|---------------|
| DEVICE | | | | | | |
| V_I | Input voltage range | | 2.4 | | 5.5 | V |
| I_Q | Operating quiescent current | $V_I = 2.8\ \text{V}$, $EN = V_I$, $SCLK = DATA = VROM = GND$, No load | | 50 | 120 | μA |
| I_{SD} | Shutdown supply current | $V_I = 2.8\ \text{V}$, $EN = GND$, $SCLK = DATA = VROM = GND$ | | | 1 | μA |
| f_{max} | Maximum operating frequency | | 320 | 400 | 520 | kHz |
| V_{UVLO} | Under-voltage lockout threshold | $V_I = 0\ \text{V}$ to $3.6\ \text{V}$ | 2.1 | 2.3 | 2.5 | V |
| | | $V_I = 3.6\ \text{V}$ to $0\ \text{V}$ | 2.0 | 2.2 | 2.4 | |
| | Hysteresis | | 30 | 100 | | mV |
| LOGIC SECTION | | | | | | |
| V_{IH} | EN/CLK/DATA high level input voltage | $V_I = 2.4\ \text{V}$ to $3.5\ \text{V}$ | 1.3 | | | V |
| | | $V_I = 3.5\ \text{V}$ to $5.5\ \text{V}$ | 1.5 | | | |
| V_{IL} | EN/CLK/DATA low level input voltage | | | | 0.4 | V |
| I_{IH} / I_{IL} | Logic input current | $EN = GND$ or V_I | | 0.01 | 0.1 | μA |
| TPS65110 OUTPUT (V_{CC}, V_{DD}, V_{SS}) | | | | | | |
| V_{CC} | V_{CC} Output DC voltage range | $V_I = 2.8\ \text{V}$, $I_{VCC} = 5\ \text{mA}$ | 3.25 | 3.3 | 3.35 | V |
| I_{VCC} | V_{CC} Output current | $I_{VDD} = 2\ \text{mA}$, $I_{VSS} = 1\ \text{mA}$ | 16 | | | mA |
| $V_{RIPPLEC}$ | V_{CC} Output voltage ripple | $I_{VCC} = 5\ \text{mA}$ | | 5 | | mV |
| V_{REGC} | V_{CC} Line regulation | $V_I = 2.4\ \text{V}$ to $5.5\ \text{V}$ | | 0.1 | 0.5 | %/V |
| L_{REGC} | V_{CC} Load regulation | $V_I = 2.8\ \text{V}$, $I_{VCC} = \text{no load to } 10\ \text{mA}$ | | 0.3 | 1 | % |
| t_{rC} | V_{CC} Rise time | 10% to 90%, no load | | 100 | | μs |
| t_{fC} | V_{CC} Fall time | 90% to 10%, no load | | 6 | | mS |
| | V_{CC} Efficiency | V_I to V_{CC} , $V_{CC} = 3.3\ \text{V}$, $I_{VCC} = 1\ \text{mA}$ | | 84% | | |
| | | V_I to V_{CC} , $V_{CC} = 3.3\ \text{V}$, $I_{VCC} = 10\ \text{mA}$ | | 86% | | |
| V_{DD} | V_{DD} Output DC voltage range | $V_{CC} = 3.3\ \text{V}$, $I_{VDD} = 1.0\ \text{mA}$, V_{DD} boost = x3 | 7.27 | 7.5 | 7.73 | V |
| I_{VDD} | V_{DD} Output current | $V_{CC} = 3.3\ \text{V}$ | 2 | | | mA |
| $V_{RIPPLED}$ | V_{DD} Output voltage ripple | $I_{VDD} = 1\ \text{mA}$ | | 7 | | mV |
| t_{rD} | V_{DD} Rise time | 10% to 90%, no load | | 1.4 | | mS |
| t_{fD} | V_{DD} Fall time | 90% to 10%, no load | | 2.4 | | mS |
| | V_{DD} Efficiency | V_{CC} to V_{DD} , $V_{CC} = 3.3\ \text{V}$, $V_{DD} = 7.5\ \text{V}$, $I_{VDD} = 0.2\ \text{mA}$ | | 70% | | |
| | | V_{CC} to V_{DD} , $V_{CC} = 3.3\ \text{V}$, $V_{DD} = 7.5\ \text{V}$, $I_{VDD} = 2\ \text{mA}$ | | 70% | | |
| V_{SS} | V_{SS} Output DC voltage range | $V_{CC} = 3.3\ \text{V}$, $I_{VSS} = 0.2\ \text{mA}$ | -2.78 | -2.7 | -2.62 | V |
| I_{VSS} | V_{SS} Output current | $V_{CC} = 3.3\ \text{V}$ | 1 | | | mA |
| $V_{RIPPLES}$ | V_{SS} Output voltage ripple | $I_{VSS} = 0.2\ \text{mA}$ | | 3 | | mV |
| t_{rS} | V_{SS} Rise time | 10% to 90%, no load | | 220 | | μs |
| t_{fS} | V_{SS} Fall time | 90% to 10%, no load | | 2 | | mS |
| | V_{SS} Efficiency | V_{CC} to V_{SS} , $V_{CC} = 3.3\ \text{V}$, $V_{SS} = -2.8\ \text{V}$, $I_{VSS} = 0.2\ \text{mA}$ | | 82% | | |
| | | V_{CC} to V_{SS} , $V_{CC} = 3.3\ \text{V}$, $V_{SS} = -2.8\ \text{V}$, $I_{VSS} = 1\ \text{mA}$ | | 82% | | |

ELECTRICAL CHARACTERISTICS Continued

over recommended free-air temperature, typical at an ambient temperature of 25°C, at $C_C1=C_C2=C_C3=0.22\ \mu\text{F}$, $C_D1=C_D2=C_D3=C_S=0.1\ \mu\text{F}$, $C_{CO}=C_{SO}=2.2\ \mu\text{F}$, $C_{DO}=1.0\ \mu\text{F}$, $V_I=3.6\ \text{V}$, and default output voltages (unless otherwise noted)

| TPS65111 OUTPUT (V_{CC} , V_{DD} , V_{SS}) | | | | | | |
|--|----------------------------------|--|-------|------|-------|---------------|
| V_{CC} | V_{CC} Output dc voltage range | $V_I = 3.6\ \text{V}$, $I_{VCC} = 5\ \text{mA}$ | 4.925 | 5.0 | 5.075 | V |
| I_{VCC} | Maximum V_{CC} output current | $I_{VDD} = 2\ \text{mA}$, $I_{VSS} = 1\ \text{mA}$ | 16 | | | mA |
| $V_{RIPPLEC}$ | V_{CC} Output voltage ripple | $I_{VCC} = 5\ \text{mA}$ | | 5 | | mV |
| V_{REGC} | V_{CC} Line regulation | $V_I = 2.7\ \text{V}$ to $5.5\ \text{V}$ | | 0.1 | 0.5 | %/V |
| L_{REGC} | V_{CC} Load regulation | $V_I = 3.6\ \text{V}$, $I_{VCC} = \text{no load to } 10\ \text{mA}$ | | 0.3 | 1 | % |
| t_{rC} | V_{CC} Rise time | 10% to 90%, no load | | 200 | | μS |
| t_{fC} | V_{CC} Fall time | 90% to 10%, no load | | 9 | | mS |
| | V_{CC} Efficiency | V_I to V_{CC} , $V_{CC} = 5.0\ \text{V}$, $I_{VCC} = 1\ \text{mA}$ | | 88% | | |
| | | V_I to V_{CC} , $V_{CC} = 5.0\ \text{V}$, $I_{VCC} = 10\ \text{mA}$ | | 90% | | |
| V_{DD} | V_{DD} Output dc voltage range | $V_{CC} = 5.0\ \text{V}$, $I_{VDD} = 1.0\ \text{mA}$, V_{DD} boost = x2 | 8.73 | 9.0 | 9.27 | V |
| I_{VDD} | Maximum V_{DD} output current | $V_{CC} = 5.0\ \text{V}$ | 2 | | | mA |
| $V_{RIPPLED}$ | V_{DD} Output voltage ripple | $I_{VDD} = 1\ \text{mA}$ | | 8 | | mV |
| t_{rD} | V_{DD} Rise time | 10% to 90%, no load | | 1.8 | | mS |
| t_{fD} | V_{DD} Fall time | 90% to 10%, no load | | 3 | | mS |
| | V_{DD} Efficiency | V_{CC} to V_{DD} , $V_{CC} = 5.0\ \text{V}$, $V_{DD} = 9.0\ \text{V}$, $I_{VDD} = 0.2\ \text{mA}$ | | 87% | | |
| | | V_{CC} to V_{DD} , $V_{CC} = 5.0\ \text{V}$, $V_{DD} = 9.0\ \text{V}$, $I_{VDD} = 2\ \text{mA}$ | | | 88% | |
| V_{SS} | V_{SS} Output dc voltage range | $V_{CC} = 5.0\ \text{V}$, $I_{VSS} = 0.2\ \text{mA}$ | -3.09 | -3.0 | -2.91 | V |
| I_{VSS} | Maximum V_{SS} output current | $V_{CC} = 5.0\ \text{V}$ | 1 | | | mA |
| $V_{RIPPLES}$ | V_{SS} Output voltage ripple | $I_{VSS} = 0.2\ \text{mA}$ | | 3 | | mV |
| t_{rS} | V_{SS} Rise time | 10% to 90%, no load | | 250 | | μS |
| t_{fS} | V_{SS} Fall time | 90% to 10%, no load | | 2.4 | | mS |
| | V_{SS} Efficiency | V_{CC} to V_{SS} , $V_{CC} = 5.0\ \text{V}$, $V_{SS} = -3.0\ \text{V}$, $I_{VSS} = 0.2\ \text{mA}$ | | 58% | | |
| | | V_{CC} to V_{SS} , $V_{CC} = 5.0\ \text{V}$, $V_{SS} = -3.0\ \text{V}$, $I_{VSS} = 1\ \text{mA}$ | | | 58% | |

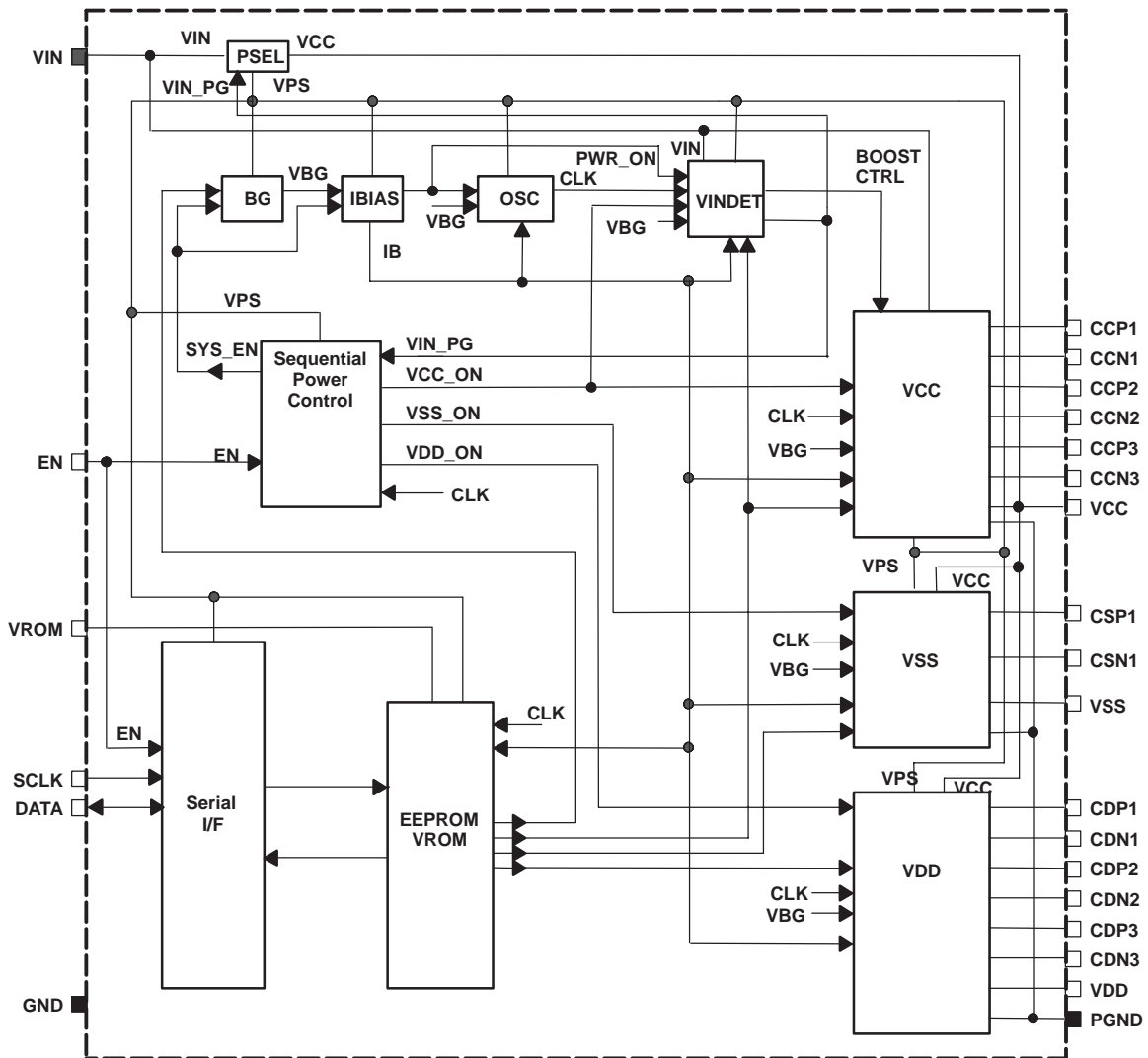
PIN ASSIGNMENTS



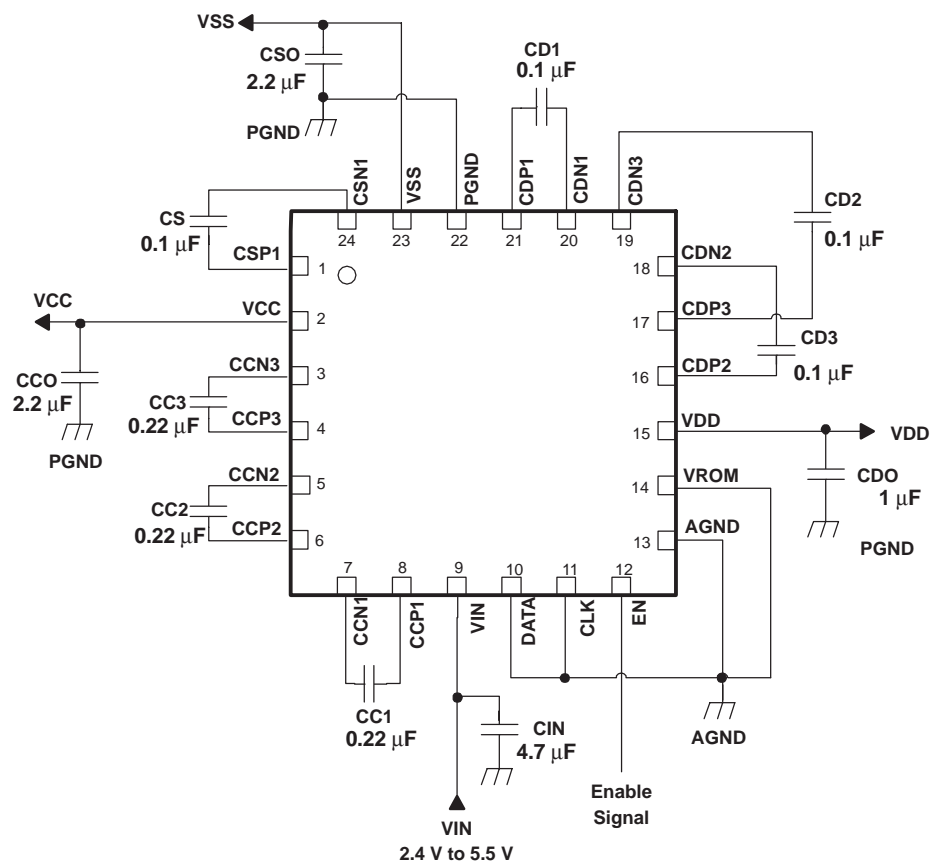
Terminal Functions

| TERMINAL | | DESCRIPTION |
|----------|------|---|
| NO. | NAME | |
| 1 | CSP1 | VSS Positive terminal for CS |
| 2 | VCC | VCC Charge pump output |
| 3 | CCN3 | VCC Negative terminal for CC3 |
| 4 | CCP3 | VCC Positive terminal for CC3 |
| 5 | CCN2 | VCC Negative terminal for CC2 |
| 6 | CCP2 | VCC Positive terminal for CC2 |
| 7 | CCN1 | VCC Negative terminal for CC1 |
| 8 | CCP1 | VCC Positive terminal for CC1 |
| 9 | VIN | Input supply voltage |
| 10 | DATA | I ² C serial data input |
| 11 | CLK | I ² C serial clock input |
| 12 | EN | Power on/off enable logic input (H : active / L : shutdown) |
| 13 | AGND | Analog GND |
| 14 | VROM | EEPROM power supply |
| 15 | VDD | VDD Charge pump output |
| 16 | CDP2 | VDD Positive terminal for CD2 |
| 17 | CDP3 | VDD Positive terminal for CD3 |
| 18 | CDN2 | VDD Negative terminal for CD2 |
| 19 | CDN3 | VDD Negative terminal for CD3 |
| 20 | CDN1 | VDD Negative terminal for CD1 |
| 21 | CDP1 | VDD Positive terminal for CD1 |
| 22 | PGND | Power GND |
| 23 | VSS | VSS Charge pump output |
| 24 | CSN1 | VSS Negative terminal for CS |

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



TYPICAL CHARACTERISTICS

VCC EFFICIENCY

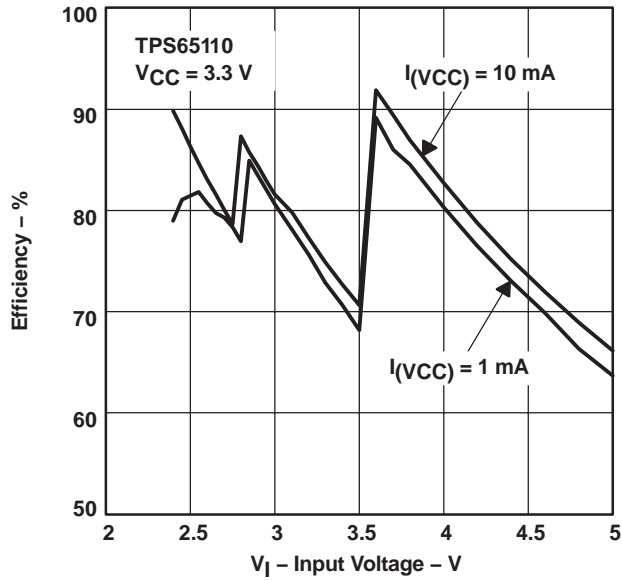


Figure 1

VCC EFFICIENCY

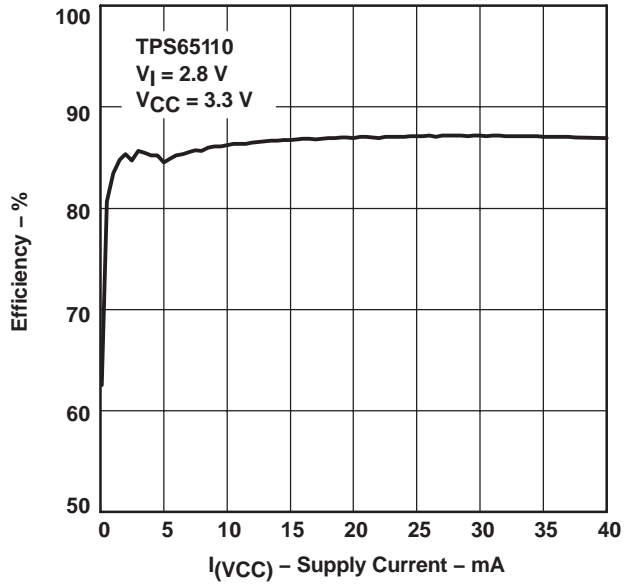


Figure 2

VCC LOAD REGULATION

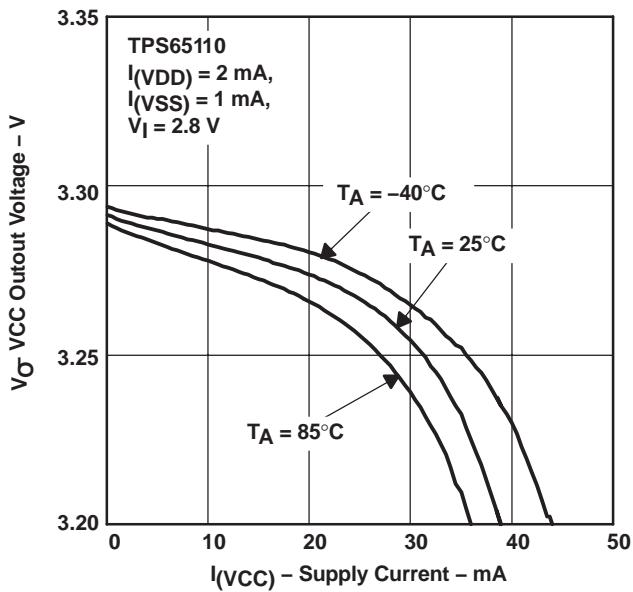


Figure 3

VCC LOAD REGULATION

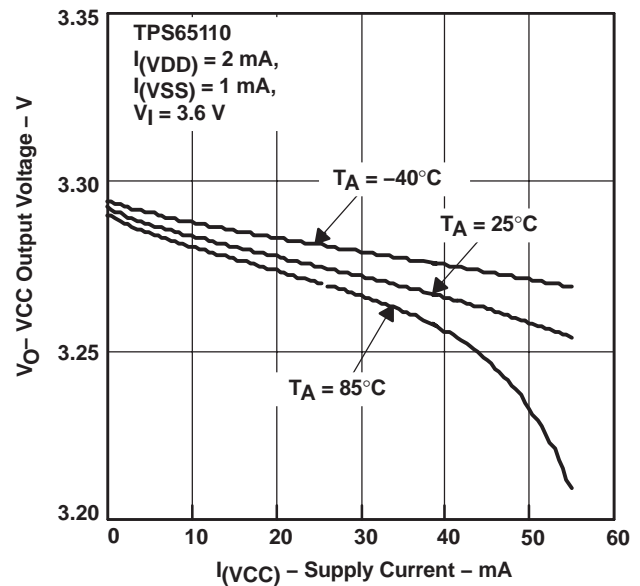


Figure 4

VDD LOAD REGULATION

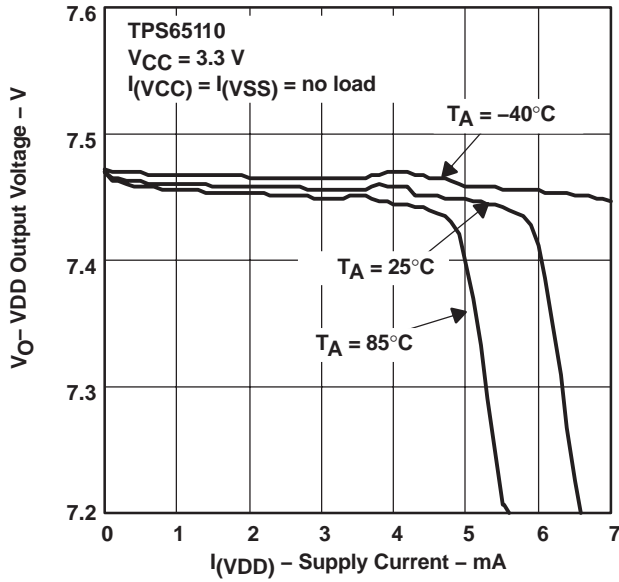


Figure 5

VSS LOAD REGULATION

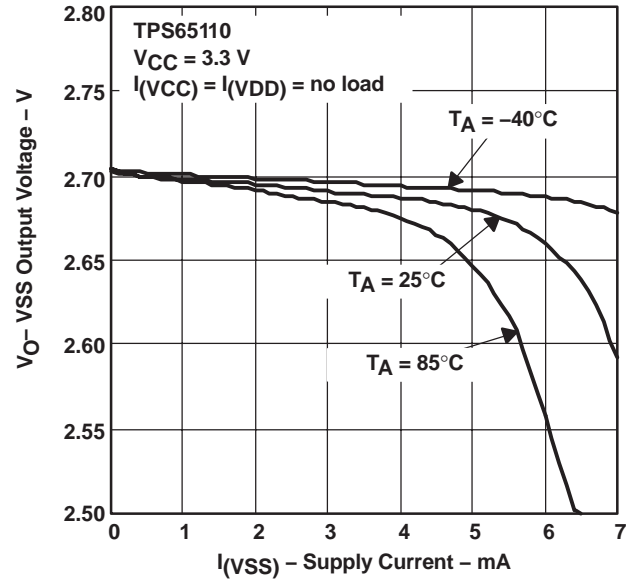


Figure 6

MAXIMUM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

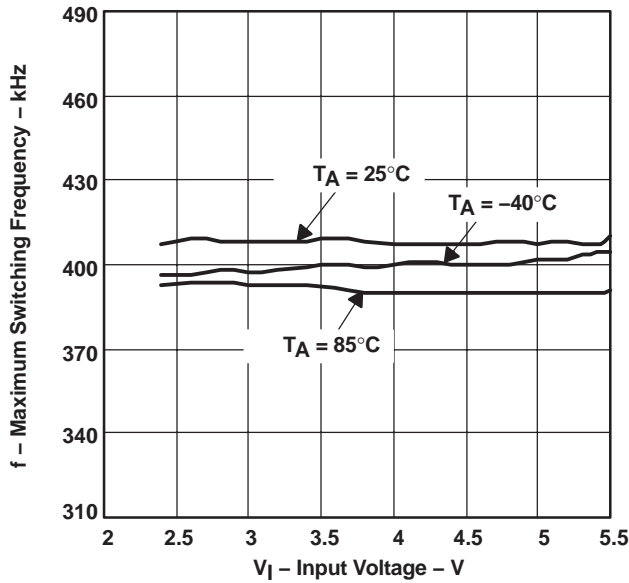


Figure 7

QUIESCENT CURRENT
vs
INPUT VOLTAGE

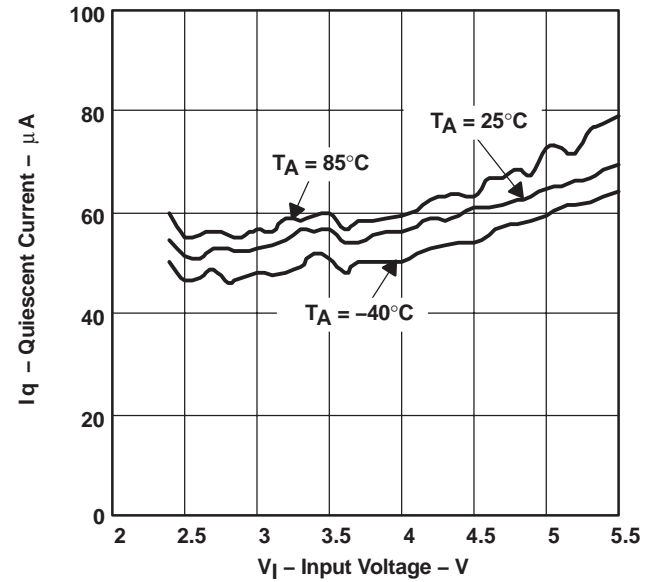
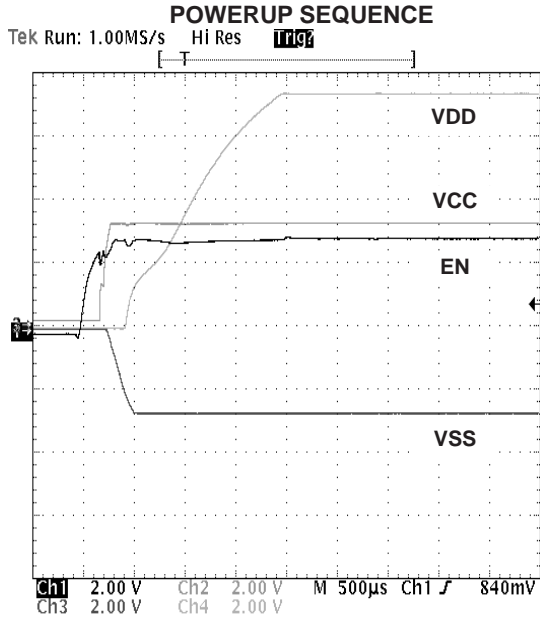
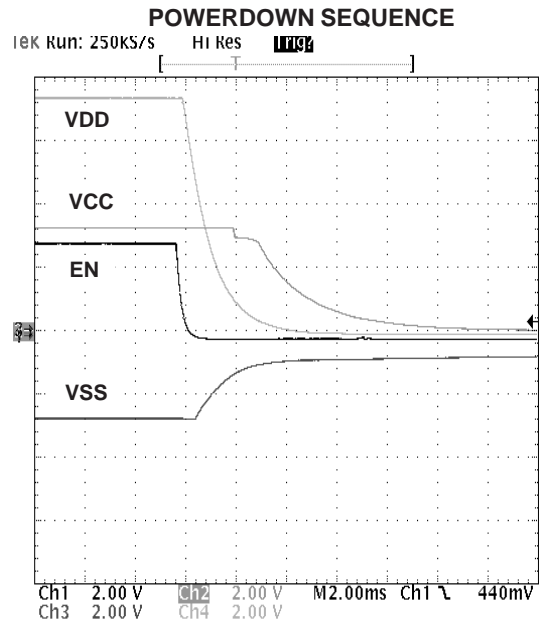


Figure 8



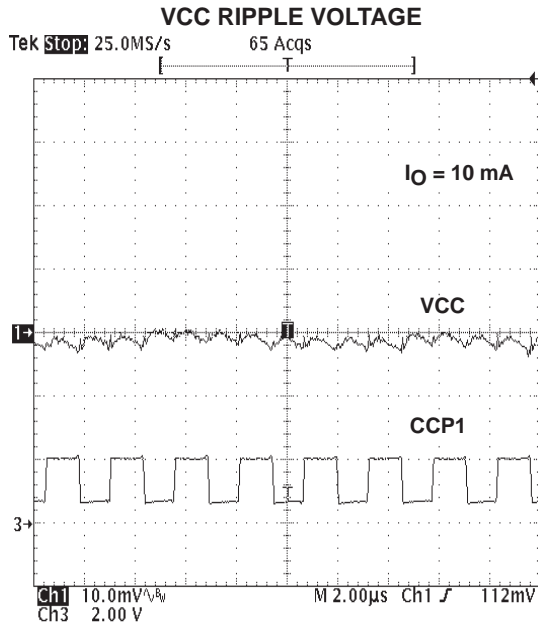
($V_I = 3.0\text{ V}$, $V_{CC} = 3.3\text{ V}$, $V_{DD} = 7.5\text{ V}$, $V_{SS} = -2.7\text{ V}$, $V_{DDBOOST} = \times 3$, No load, $C_{C1/2/3} = 0.22\text{ }\mu\text{F}$, $C_{CO} = 2.2\text{ }\mu\text{F}$)

Figure 9



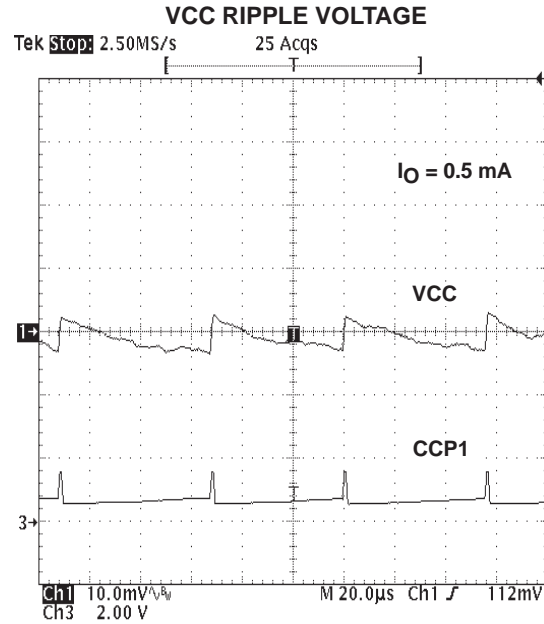
($V_I = 3.0\text{ V}$, $V_{CC} = 3.3\text{ V}$, $V_{DD} = 7.5\text{ V}$, $V_{SS} = -2.7\text{ V}$, $V_{DDBOOST} = \times 3$, No load, $C_{C1/2/3} = 0.22\text{ }\mu\text{F}$, $C_{CO} = 2.2\text{ }\mu\text{F}$)

Figure 10



($V_I = 2.7\text{ V}$, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{C1/2/3} = 0.1\text{ }\mu\text{F}$, $C_{CO} = 2.2\text{ }\mu\text{F}$)

Figure 11



($V_I = 2.7\text{ V}$, $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, $C_{C1/2/3} = 0.1\text{ }\mu\text{F}$, $C_{CO} = 2.2\text{ }\mu\text{F}$)

Figure 12

DETAILED DESCRIPTION

VCC Charge Pump

The VCC output provides a very high efficiency, regulated, dc/dc conversion through a wide input range by supporting x1.0, x1.33, x1.5, and x2.0 boost charge pump operation. TPS65110 automatically sets the boost ratio based on input and output voltage conditions. For example, when the input voltage from a battery becomes lower, the device automatically increases the boost ratio from x1.33 to x1.5. In a fixed input voltage mode, the device provides for higher conversion efficiency; for example, in the case of 2.8 V to 3.3 V conversion or 2.8 V to 5.0 V conversion. In this case, the VCC charge pump can enter into a *SKIP* mode operation in order to maintain the efficiency of a low load condition. The highest frequency of the charge pump is 400 kHz (typ). The charge pump operates by using higher frequencies in the heavier load current conditions, and decreases the frequency in the lighter load conditions. Maximum output current and operating frequency characteristics are dependent on external conditions such as the flying capacitor, output capacitor, and ambient temperature range.

| VCC[V] | VIN [V] | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------|---------|-----|-----|-------|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|-----|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|--|
| | 2.4 | 2.5 | 2.6 | 2.7 | 2.8 | 2.9 | 3.0 | 3.1 | 3.2 | 3.3 | 3.4 | 3.5 | 3.6 | 3.7 | 3.8 | 3.9 | 4.0 | 4.1 | 4.2 | 4.4 | 4.6 | 4.8 | 5.0 | 5.2 | 5.4 | 5.5 | |
| 3.3 | x1.5 | | | x1.33 | | | | | | | | | x1 | | | | | | | | | | | | | | |
| 5.0 | NA | | | x2 | | | | | | | | | x1.5 | | | | x1.33 | | | | | | | x1 | | | |

NOTE: Gray portion is HYSTERESIS.

Of importance, the VCC charge pump is also used as the power source for the VDD and VSS charge pumps. Therefore, consider a case where the VDD charge pump's output current is required to be 2mA, and the boost ratio is x3. With this condition, the required (additional) current for the VCC output is slightly more than 6 mA. If the VSS charge pump output current requirement is 1 mA, then the (additional) required current from VCC is another 1 mA. (Note: the VCC charge pump maintains a minimum of 16-mA output capability in addition to the loads required to support the VDD and VSS charge pumps under the recommended conditions.)

VDD Charge Pump

The power source for the VDD charge pump is the VCC charge pump. The output voltage and boost ratio of the VDD charge pump are fixed at either a 7.5 V and x3 boost (TPS65110), or a 9.0 V and x2 boost (TPS65111). The topology of this charge pump is *SKIP mode*, and the maximum frequency is 400 kHz. Maximum output current is dependent on the flying capacitors and ambient temperature range (refer to the typical characteristics).

VSS Charge Pump

The VSS charge pump is powered from the VCC charge pump and has a fixed output voltage of either -2.7 V (TPS65110) or -3.0 V (TPS65111). The boost ratio for the VSS charge pump is fixed at x-1. The operation topology is *SKIP mode* and has a maximum frequency of 400 kHz. Maximum output current is dependent on the flying capacitor and ambient temperature range (refer to the typical characteristics).

UVLO – Under Voltage Lockout

The UVLO provides for the save operation of the device. It prevents the converter from turning on when the voltage on the VIN pin is less than the threshold voltage of UVLO. Note that although the input voltage range of the product is shown to be down to 2.4 V, the maximum threshold of the UVLO for a rising VIN is 2.5 V. Therefore, to operate down to 2.4 V, the device must first be powered by a source of more than 2.5 V.

Enable

Low logic on the EN pin forces the TPS6511x into shutdown mode. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 1 μ A in shutdown mode.

Power-Up and Power-Down Sequencing

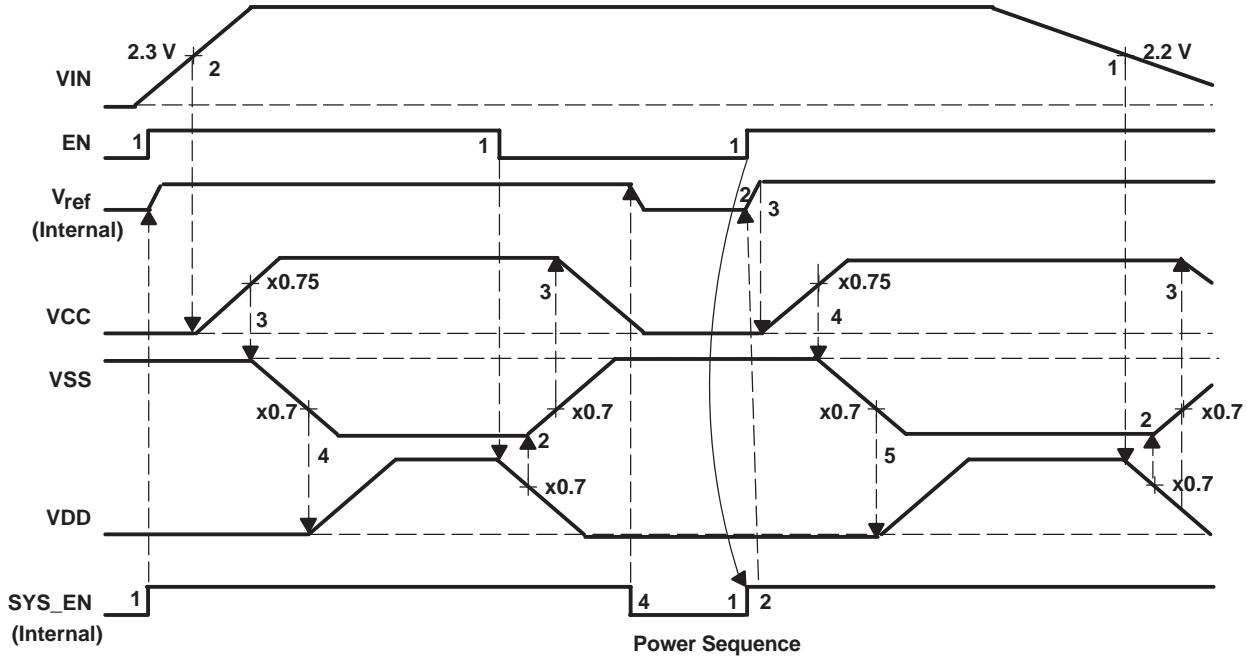
The TPS65110/11 controls power-up and power-down sequence through an enable pin. This signal should be terminated and not be left floating to prevent miss-operation.

Power-Up Sequence

When the enable pin EN is pulled high, the device starts its power on sequencing. The VCC output starts up first. When the output voltage VCC has reached 75% of its nominal value, the VSS output comes up next. When VSS has reached 75% of the nominal value, the positive output VDD finally comes up.

Power-Down Sequencing

When the enable pin EN is pulled low, the device starts its power-down sequencing. The VDD output goes down first. When the output voltage VDD has reached 70% of its nominal value, the VSS output goes down next. When VSS has reached 70% of the nominal value, the positive output VCC finally goes down. The TPS6511x ensures this power-down sequence even in the case of a sudden V_I drop.



PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| TPS65110RGE | ACTIVE | VQFN | RGE | 24 | 92 | Green (RoHS & no Sb/Br) | CU | Level-2-260C-1 YEAR |
| TPS65110RGEG3 | ACTIVE | VQFN | RGE | 24 | 92 | Green (RoHS & no Sb/Br) | CU | Level-2-260C-1 YEAR |
| TPS65110RGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS65110RGERG4 | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS65111RGE | ACTIVE | VQFN | RGE | 24 | 92 | Green (RoHS & no Sb/Br) | CU | Level-2-260C-1 YEAR |
| TPS65111RGEG4 | ACTIVE | VQFN | RGE | 24 | 92 | Green (RoHS & no Sb/Br) | CU | Level-2-260C-1 YEAR |
| TPS65111RGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| TPS65111RGERG4 | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

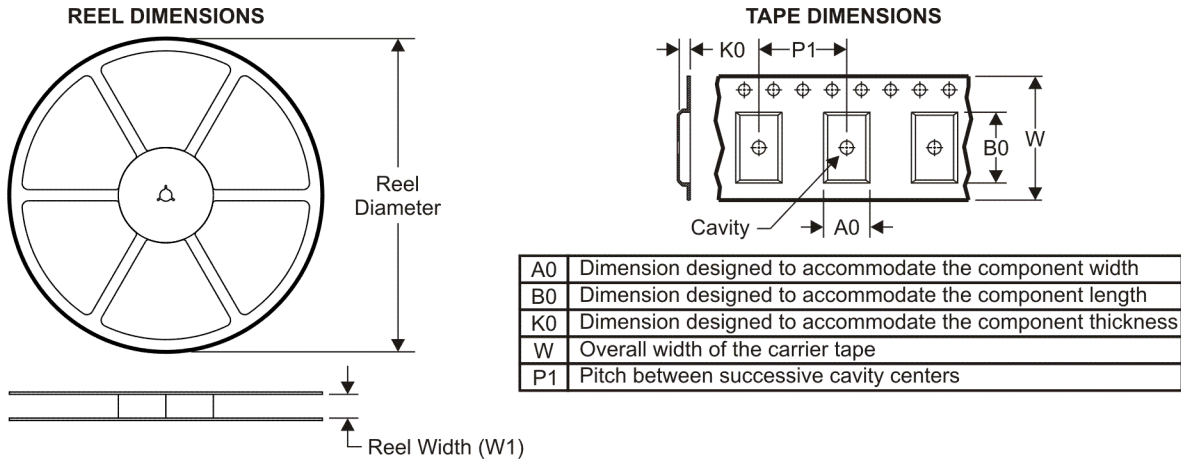
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65110RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TPS65111RGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.3 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

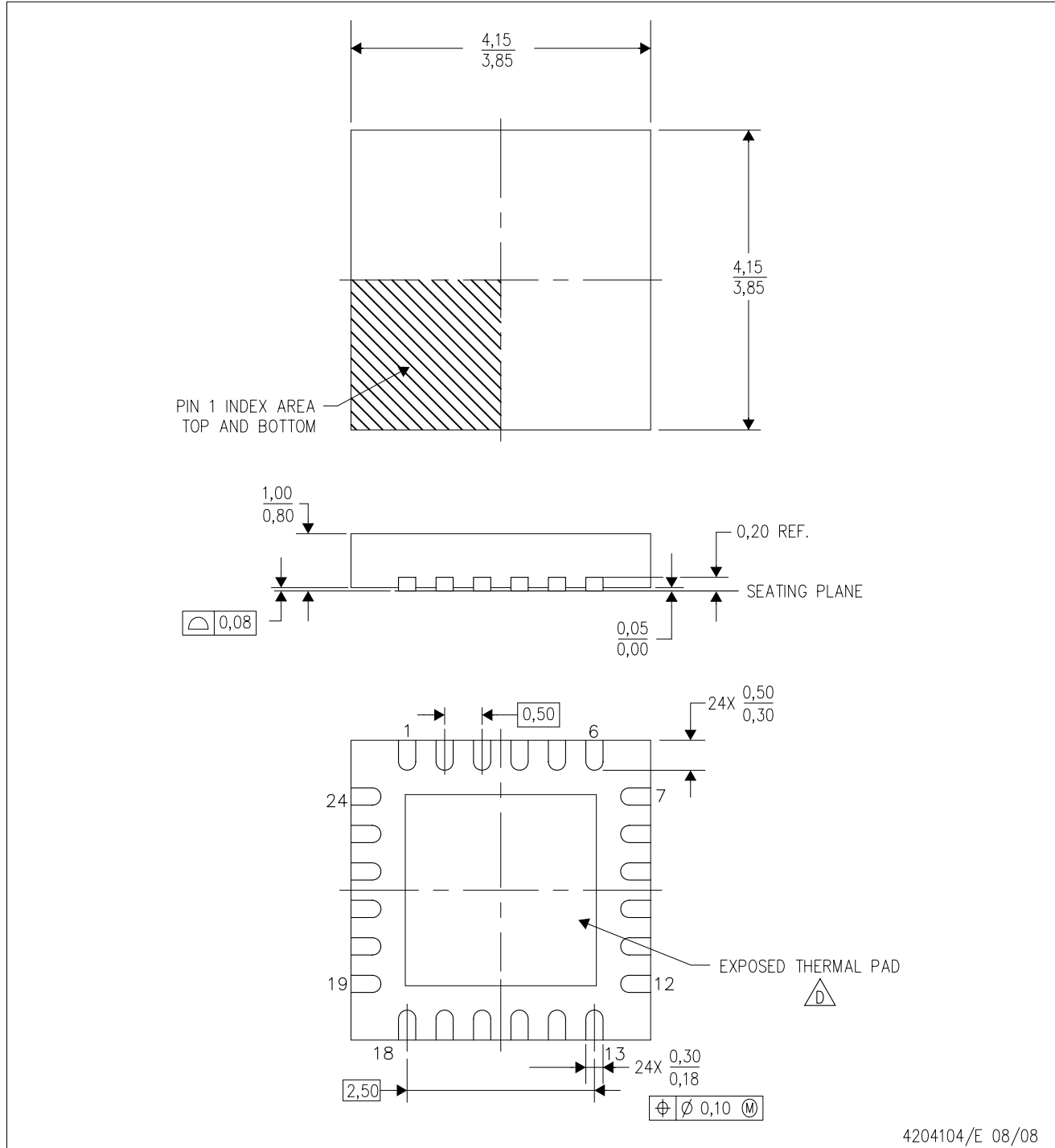



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65110RGER | VQFN | RGE | 24 | 3000 | 340.5 | 333.0 | 20.6 |
| TPS65111RGER | VQFN | RGE | 24 | 3000 | 340.5 | 333.0 | 20.6 |

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



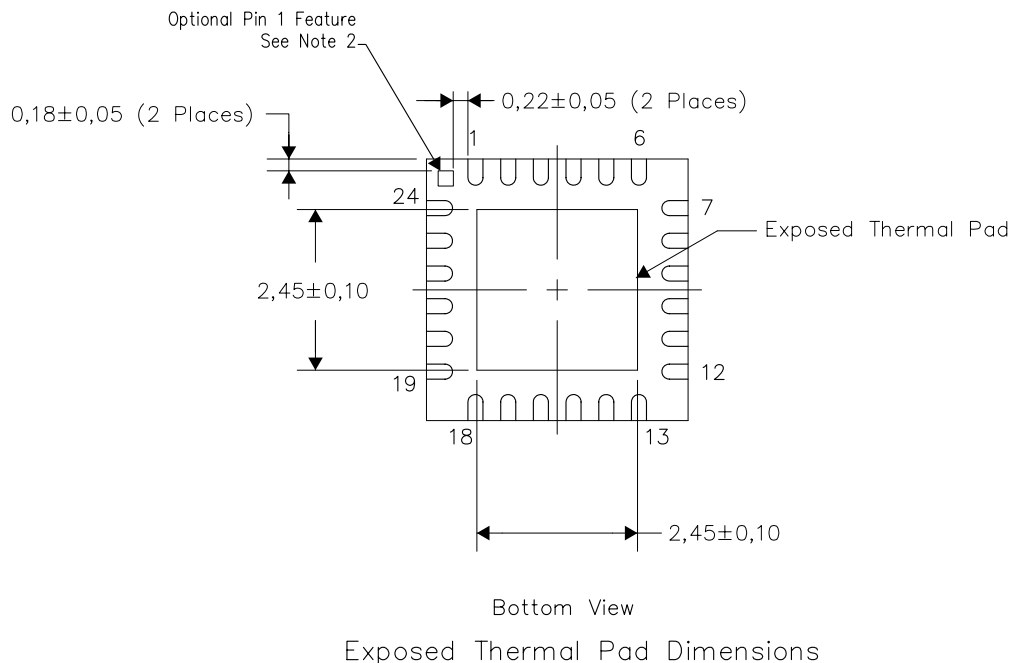
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-Leads (QFN) package configuration.
 -  The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

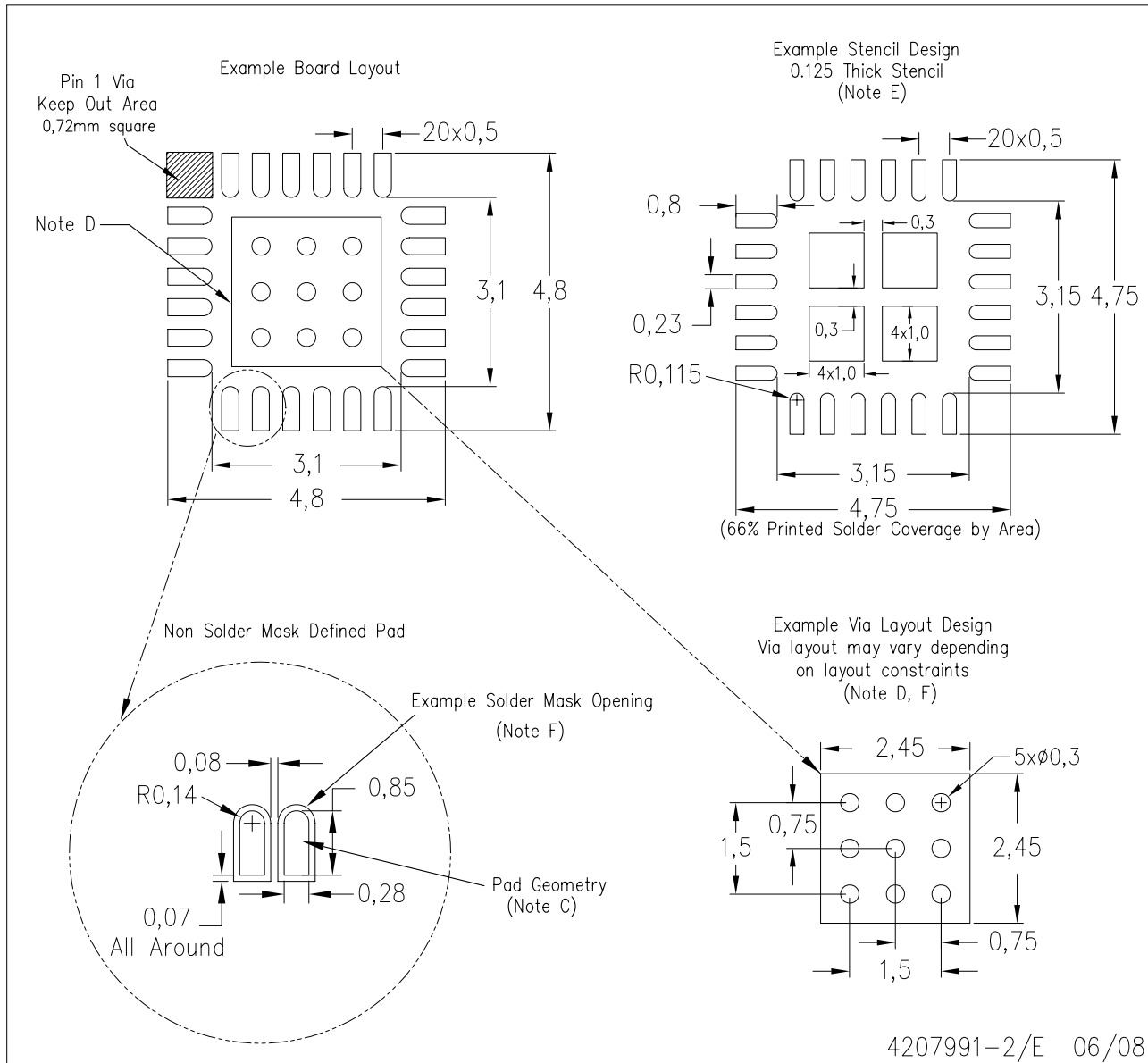
The exposed thermal pad dimensions for this package are shown in the following illustration.



NOTES:

- 1) All linear dimensions are in millimeters
- 2) The Pin 1 Identification mark is an optional feature that may be present on some devices
 In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S-PVQFN-N24)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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